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21. (New) The device according to claim 12, wherein said pattern of circuit connections includes at one of the following to interconnect said plurality of circuit devices: a signal plane, a power plane and a ground plane.
22. (New) The device according to claim 12, wherein said interconnect layer includes a power plane and a ground plane, and wherein said decoupling capacitor connects in parallel between said power and ground planes.
23. (New) The device according to claim 12, wherein said support base comprises a silicon containing substrate.
24. (New) The device according to claim 12, wherein said decoupling capacitor comprises a silicon containing dielectric material.
25. (New) The device according to claim 12, wherein said interconnecting layer comprises a plurality of aluminum containing conductive paths.
26. (New) The device according to claim 12, wherein said interconnecting layer comprises a plurality of copper containing conductive paths.
27. (New) The device according to claim 12, wherein said decoupling capacitor comprises a silicon base die decoupling capacitor.
28. (New) The device according to claim 12, said decoupling capacitor having a capacitance in the range of 1 to 1000 nf/cm².
29. (New) The device according to claim 28, said decoupling capacitor having a capacitance of approximately 50 nf/cm².
30. (New) The device according to claim 12, further comprising a plurality of decoupling capacitors mounted on said first surface.

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cond.
31. (New) The device according to claim 12, further comprises at least one resistor mounted on said first surface.
 32. (New) The device according to claim 12, wherein said plurality of circuit devices are in electrical communication with said decoupling capacitor.
 33. (New) The device according to claim 12, wherein said decoupling capacitor includes a pair of pads and said pattern of circuit connections includes a ground plane and a power plane, wherein one pad is coupled to said ground plane and the other pad is coupled to said power plane.
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